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EXAMINER

KIELIN, ERIK J

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 04/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/995,575	<b>Applicant(s)</b> YASUMOTO, TAMIHIDE	
	<b>Examiner</b> Erik Kielin	<b>Art Unit</b> 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 February 2004.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,2,5-9 and 11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,5-9 and 11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9 February 2004 has been entered.

### ***Drawings***

2. The drawings were received on 9 February 2004. These drawings are acceptable.

### ***Claim Objections***

3. Claim 9 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The limitations of claim 9 were amended into the independent claim 1 and are therefore not further limiting of claim 1.

### ***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

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5. Claims 1, 2, 4, and 5-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Independent claims 1 and 5 were amended to include the limitation that the oxidizing of the wiring occurs “for at most 20 seconds.” This is not supported by the original specification which only provides a single example in passing and indicates that the period of time is 20 seconds --not “for at most 20 seconds.” Accordingly this is new matter. In this regard, MPEP 2163.05 (III) states,

“With respect to **changing numerical range limitations**, the analysis must take into account which ranges one skilled in the art would consider inherently supported by the discussion in the original disclosure. In the decision in *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976), the ranges described in the original specification included a range of “25%-60%” and specific examples of “36%” and “50%.” A corresponding new claim limitation to “at least 35%” did not meet the description requirement because the phrase “at least” had no upper limit and caused the claim to read literally on embodiments outside the “25% to 60%” range, however a limitation to “between 35% and 60%” did meet the description requirement.

See also *Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1328, 56 USPQ2d 1481, 1487 (Fed. Cir. 2000) (“the specification does not clearly disclose to the skilled artisan that the inventors \* \* \* considered the [ ] ratio to be part of their invention \* \* \*. There is therefore no force to Purdue’s argument that the written description requirement was satisfied because the disclosure revealed a broad invention from which the [later-filed] claims carved out a patentable portion”). Compare *Union Oil of Cal. v. Atlantic Richfield Co.*, 208 F.3d 989, 997, 54 USPQ2d 1227, 1232-33 (Fed. Cir. 2000) (Description in terms of ranges of chemical properties which work in combination with ranges of other chemical properties to produce an automotive gasoline that reduces emissions was found to provide an adequate written description even though the exact chemical components of each combination were not disclosed and the specification did not disclose any distinct embodiments corresponding to any claim at issue. “[T]he Patent

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Act and this court's case law require only sufficient description to show one of skill in the...art that the inventor possessed the claimed invention at the time of filing."")"

***Claim Rejections - 35 USC § 102***

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 11 is rejected under 35 U.S.C. 102(e) as being unpatentable over US 6,255,179 B1 (Cantell et al.).

Regarding claim 11, **Cantell** discloses a method for manufacturing a semiconductor device, comprising the steps of:

forming a wiring comprising silicon on a surface of a semiconductor substrate (col. 5, lines 9-17);

covering part of the wiring with a resist pattern (col. 1, lines 27-38; col. 5, lines 14-15);

implanting ions into the wiring using the resist pattern as a mask to form a carbon containing region in a surface layer of the wiring in the vicinity of an edge of the resist pattern (col. 3, lines 36-41; col. 1, lines 52-55);

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removing the resist pattern (col. 1, lines 47-52);

oxidizing the surface layer of the wiring to form an oxide film so that the carbon containing region is merged into the oxide film using a rapid thermal processing apparatus, a plasma processing apparatus such as the Model 5000 CVD chamber from Applied Materials (col. 3, lines 55-57; paragraph bridging cols. 3 and 4; col. 4, lines 5-15);

removing the oxidized portion of the wiring to remove the carbon contamination in the silicon wiring generated from "knocked-on carbon from the mask" during the implanting step (col. 4, lines 5-15; col. 5, lines 9-16); and

forming a metal silicide film on a surface of the wiring by causing reaction between a surface layer of the wiring and a refractory metal which reacts with silicon to form silicide (col. 4, lines 45 to col. 5, line 16).

### ***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1, 2, 4, 9 and 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,255,179 B1 (**Cantell et al.**) in view of US 5,593,924 (**Apte et al.**) and excerpts from **Van Zant, Microchip Fabrication**, 4<sup>th</sup> ed, McGraw-Hill: New York, 2000, pp. 34, 172-173, 179-182.

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Regarding claims 1, 2, and 4, **Cantell** discloses a method of manufacturing a semiconductor device comprising,

forming a wiring comprising silicon on a surface of a semiconductor substrate (col. 5, lines 9-17);

covering part of the wiring with a resist pattern (col. 1, lines 27-38; col. 5, lines 14-15);

implanting ions into the wiring using the resist pattern as a mask (col. 1, lines 27-38; col. 5, lines 14-15);

removing the resist pattern (col. 1, lines 47-52);

thinning the wiring by removing a surface of the wiring to a depth of 10 to 200 Å (1 to 20 nm), more preferably 20-80 Å (2 to 8 nm) to remove the carbon contamination in the silicon wiring generated from “knocked-on carbon from the mask” during the implanting step (col. 4, lines 5-25; col. 5, lines 9-16); and

forming a metal silicide on a surface of the wiring by depositing cobalt or titanium metal on the silicon and then reacting the metal with the silicon by annealing (col. 4, lines 45 to col. 5, line 16),

wherein the wiring thinning step comprises the steps of:

oxidizing the wiring beginning on an upper surface thereof down to a predetermined depth (col. 3, lines 55-57); and

removing an oxidized section of the wiring oxidized in the oxidizing step (col. 4, lines 5-15; col. 5, lines 9-16).

Regarding claims 5, 6, and 8, **Cantell** discloses a method of manufacturing a semiconductor device comprising,

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forming a wiring comprising silicon on a surface of a semiconductor substrate (col. 5, lines 9-17);

covering part of the wiring with a resist pattern (col. 1, lines 27-38; col. 5, lines 14-15);

implanting ions into the wiring using the resist pattern as a mask (col. 1, lines 27-38; col. 5, lines 14-15);

removing the resist pattern (col. 1, lines 47-52);

oxidizing the wiring beginning on an upper surface thereof down to a depth of 10 to 200 Å, more preferably 15-30 Å and (col. 3, lines 55-57);

removing the oxidized portion of the wiring to remove the carbon contamination in the silicon wiring generated from "knocked-on carbon from the mask" during the implanting step (col. 4, lines 5-15; col. 5, lines 9-16); and

forming a metal silicide on a surface of the wiring by depositing cobalt or titanium metal on the silicon and then reacting the metal with the silicon by annealing (col. 4, lines 45 to col. 5, line 16).

As applied to independent claims 1 and 5 above, **Cantell** does not indicate that the wire oxidizing step is performed in an atmosphere of hydrogen and oxygen for no more than 20 seconds. **Cantell** does, however, suggest that other oxidation methods may be used (col. 3, lines 55-61).

**Van Zant** teaches (p. 181) that rapid thermal oxidation can be carried out using steam, and that steam is beneficially cleaner, and the oxidation process better controlled, by combusting hydrogen and oxygen (paragraph bridging pp. 172-173).




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It would have been obvious for one of ordinary skill in the art, at the time of the invention to use an atmosphere of hydrogen and oxygen to form the oxidizing atmosphere, as taught in **Van Zant**, to oxidize the wiring of **Cantell**, because the intention in **Cantell** is remove contamination and **Van Zant** teaches using H<sub>2</sub> and O<sub>2</sub> is preferred for at least the **better cleanliness** and control of the oxidation process. Further in this regard, it is noted that the instant specification indicates that there exists nothing critical about the method of oxidizing the wiring layer stating instead at page 10, lines 16-20,

“In the **embodiment**, wet oxidation is employed to oxidize the wiring 42 using the RTP apparatus in the process shown in FIG. 2C. However, **another method may also be used**. For example, the substrate may be **dipped into an oxidizing agent** or **an electric furnace** may be used in place of the RTP apparatus.” (Emphasis added.)

Accordingly, so long as the silicon wiring is oxidized sufficiently to incorporate the contamination, the method of oxidation of the wiring cannot be considered novel in the absence of an unexpected result. Yet, the instant specification teaches away from any such unexpected result.

Although the time of 20 seconds is not taught, it would be a matter of routine optimization to perform the oxidation of the wiring for the time sufficient to incorporate the carbon contamination into the formed oxide, as expressly indicated in **Cantell**. There exists no evidence of unexpected results for the period of 20 seconds. Inasmuch as **Cantell** is performing the oxidation for the **exact same purpose** as in the instant application --specifically removal of carbon contamination prior to silicide formation-- the period of time for oxidation cannot be considered novel in the absence of evidence of unexpected results.




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In this regard, it has been held that “[n]ormally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed **produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...** such ranges are termed ‘critical ranges’ and the **applicant has the burden of proving such criticality** .... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” *In re Aller* 105 USPQ233, 255 (CCPA 1955). See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sold* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

Then as applied to independent claims 1 and 5 above, the only difference is that **Cantell** does not indicate that titanium nitride (TiN) is deposited over the metal layer to form the metal silicide.

**Apte** teaches that it is known in the art to form a TiN cap layer over a cobalt metal layer before reacting the metal layer with the silicon to reduce the variability in the sheet resistance of the cobalt silicide.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use a TiN cap layer over the silicide-forming metal layer of **Cantell** in order to produce a silicide wiring having a uniform sheet resistance, as taught to be known by **Apte**.



Also as applied to independent claims 1 and 5 above, **Cantell** does not indicate that the implanted ions may be arsenic, but does indicate the n-type dopant is used.

The basic textbook of **Van Zant** teaches that arsenic is a notoriously well-known n-type dopant (p. 34).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use arsenic because **Cantell** states to use an n-type dopant and **Van Zant** teaches that arsenic is an n-type dopant.

Moreover, the selection of a known material based on its suitability for its intended use is *prima facie* obvious. (See MPEP 2144.07.)

As applied to all of the above claims, **Cantell** does not use the terminology that the apparatus used to oxidize the wiring is a rapid thermal processing apparatus. This limitation is believed to have little patentable weight because it has been held that to be entitled to weight in method claims, the recited structure limitations therein must affect the method in a manipulative sense, and not amount to the mere claiming of a use of a particular structure. See *Ex parte Pfeiffer*, 1962, C.D. 408 (1961). In the instant case, it appears that the claims merely claim the use of a structure, i.e. the rapid thermal processing apparatus.

If it is thought that the “using a rapid thermal processing apparatus” has patentable weight, and if it is thought that the processing apparatus of **Cantell** is not somehow a rapid thermal processing apparatus, then this may be a difference.

The basic textbook of **Van Zant** teaches that rapid thermal processing is advantageous for reducing thermal budget (p. 180, first sentence).

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It would have been obvious for one of ordinary skill in the art, at the time of the invention to use a rapid thermal processing apparatus to oxidize the wiring of **Cantell** in order to beneficially reduce the thermal budget.

Regarding claim 7, it is clear that the amount of the silicon oxidized in **Cantell** is less than the depth, otherwise there would be no silicon wiring left, contrary to the teaching in **Cantell**.

#### *Response to Arguments*

10. Applicant's arguments filed 9 February 2004 have been fully considered but they are not persuasive.

Applicant's arguments are directed to the newly added limitations which are not considered novel or non-obvious for reasons indicated in the rejection of the claims above and are incorporated herein in their entirety.

#### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Erik Kielin

Primary Examiner

24 April 2004